REMARKS

The present amendment is in response to the Office Action dated July 8, 2003, where the Examiner has rejected claims 1-34 and 58-71. By the present amendment, claims 1, 12, 23, 58, 70 and 71 have been amended. Accordingly, claims 1-34 and 58-71 are pending in the present application. Reconsideration and allowance of pending claims 1-34 and 58-71 in view of the amendments and the following remarks are respectfully requested.

A. Objection to the Drawings

The drawings have been objected to by the PTO Draftsperson for containing informalities. As discussed during a telephone correspondence conducted between Mr. Jonathan Velasco of our office and Mr. Thomas Dickey of the PTO on October 8, 2003, the Examiner has agreed to defer the requirement for corrected and/or formal drawings to be filed in the present application until a Notice of Allowance is issued in the present application.

B. Objection to the Specification

Responsive to the Examiner's objection to the Abstract, applicant has amended the first paragraph of the Abstract to further recite that the pinned transfer gate "is tied to the potential of a substrate of the imager cell and is disposed between the photoreceptor and the sense node in order to transfer charge between the photoreceptor and the sense node."

Applicant respectfully submits that the Abstract now meets the guidelines set forth in MPEP §609.

C. **Rejection based on Double Patenting**

The Examiner has provisionally rejected claims 1-11 under statutory type (35 USC §101) double patenting as claiming the same invention as that of claims 1-11 of copending Application No. 09/977,444. As discussed further below, applicant has amended independent claim 1 and, as such, amended independent claim 1 and its corresponding dependent claims 2-11 specify limitations different from those specified by claims 1-11 of copending Application No. 09/977,444. Applicant respectfully submits that the provisional rejection of claims 1-11 under statutory type (35 USC §101) double patenting has been traversed.

The Examiner has further provisionally rejected claims 1-34 and 58-71 under the judicially created doctrine of double patenting as being unpatentable over claim 1 of copending Application No. 10/135,708. Along with the present amendment, applicant has submitted a terminal disclaimer to overcome the Examiner's provisional rejection under the judicially created doctrine of double patenting with respect to claim 1 of copending Application No. 10/135,708. Applicant respectfully submits that the enclosed terminal disclaimer overcomes the provisional rejection of claims 1-34 and 58-71 under the judicially created doctrine of double patenting.

D. Rejection of Claims 1-34 and 58-71 Under 35 USC §112, First Paragraph

The Examiner has rejected claims 1-34 and 58-71 under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification is such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses the rejection.

With reference to the exemplary embodiment shown in Figure 2 and the description set forth beginning on page 6, line 22 of the present application, the specification describes that the "pinned transfer gate 206 is formed from a shallow p++ implanted pinned region 219 in an n-implanted transfer region 221 in the p-type substrate 202." The specification further describes that "the pinned transfer gate 206 is disposed between the photoreceptor 204 and the sense node 208 in order to transfer charge between the photoreceptor 204 and the sense node 208. Note also that the pinned transfer region omits a transistor gate structure." Page 6, line 24 to page 7, line 2 of the present application.

With regard to "whether a "Pinned Transfer gate must be electrically tied to the substrate," the specification describes that the "pinned transfer gate is "pinned" because the p++ doped pinned region 219 is tied (or "pinned") to the potential of the substrate 202, typically ground or zero volts." Page 7, lines 6-7 of the present application. In other words, p++ doped pinned region 219 is "tied to," i.e., coupled to, the same potential that substrate 202 is tied to, such that p++ doped pinned region 219 and substrate 202 are

coupled to the same potential. As is known in the art, there are numerous ways for connecting a substrate, such as substrate 202, and a substrate region, such as p++ doped pinned region 219, to the same potential.

With regard to element 210, applicant notes that element 210 is identified in the present application as reset transistor 210, not as an "insulated, clocked transfer gate" as understood by the Examiner. See, for example, page 6, line 14 and page 8, line 14 of the present application. To clarify, the description set forth on page 7, lines 1-5 of the present application describes that "the pinned transfer region omits a transistor gate structure." In other words, pinned transfer gate 206 does not rely upon a convention transistor gate structure, such as photoreceptor readout gate 216 for photoreceptor 204, in order to transfer charge. Thus, the description set forth on page 7, lines 1-5 of the present application does not relate to whether reset transistor 210 is required or not required, but rather points out that pinned transfer gate 206 does not have a conventional transistor gate structure. For these reasons, applicant respectfully submits that the fabrication of pinned transfer gate 206 and its associated operation is clearly shown and described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully submits that the rejection of claims 1-34 and 58-71 under 35 USC §112, first paragraph, has been traversed.

E. Rejection of Claims 1-8 Under 35 USC §102

Claims 1 and 5-8.

The Examiner has rejected claims 1 and 5-8 under 35 USC §102(e) as being anticipated by U.S. patent application publication 2002/0121656 to Guidash ("Guidash '656"). For the reasons discussed below, applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Guidash '656. However, applicant reserves the right to provide declarations and/or documents under 37 CFR §1.131 to "swear behind" the effective filing date of Guidash '656.

Subject to applicant's reserved right to establish priority of the present invention under 37 CFR §1.131, applicant submits that the present invention, as defined by amended independent claim 1, is directed to "an imager cell including a substrate connected to a voltage," wherein the imager cell comprises "a photoreceptor; a sense node; and a pinned transfer gate disposed between the photoreceptor and the sense node, the pinned transfer gate being connected to the voltage and further being configured transfer charge between the photoreceptor and the sense node." As discussed above, a "pinned transfer gate" is tied to or coupled to the same voltage or potential as the substrate. For example, the pinned transfer gate and the substrate may both be connected to ground or zero volts. See, for example, page 7, lines 6-7 of the present application. With this unique arrangement, the pinned transfer gate is pinned to the same potential as the substrate, and, as such, does not require a conventional transistor gate structure to

transfer charge, i.e., from the photoreceptor to the sense node. See, for example, page 7, lines 2-5.

To clarify the readout operation of the present invention, applicant references the potential well diagram 214 of Figure 2 and the description set forth beginning on page 8, line 7 of the present application, wherein the specification describes that "after integration period 222, the control circuitry 114 applies the readout voltage V- to establish the readout potential well 228. Note that the readout potential well 228 is shallower than the transfer potential well 230, established by pinned transfer gate 206. As a result, electrons captured by the integration potential well 226 propagate through the transfer potential well 230 and into the sense node potential well." As pointed out above, this readout operation is achieved without requiring a transistor gate structure for the pinned transfer gate due to the unique structural arrangement employing pinned transfer gate 206, which is tied to the same potential as substrate 202 in Figure 2.

In contrast, the disclosure of Guidash '656 fails to disclose or remotely suggest a pinned transfer gate as specified by claim 1. For example, with reference to Figures 2 and 5 of Guidash '656, charge is transferred from photodiode 12 to sense node 24 by way of transfer transistor 14 (Figure 2 of Guidash '656) corresponding to transfer transistor structure 16 (Figure 5 of Guidash '656). As clearly shown in Figure 5 of Guidash '656, transfer transistor 14, by its nature, includes a transistor gate structure situated between source and drain regions 34. As such, transfer transistor 14 cannot be a pinned transfer gate as specified by claim 1, because, a pinned transfer gate does not include a transistor gate structure, as discussed above. Moreover, the gate of transfer transistor 14 (labeled

"TG" in Figure 2 of Guidash '656) is not tied to the same potential as the substrate in Guidash '656. Instead, in order transfer charge from photodiode 12 to sense node 24 in Guidash '656, a sufficient voltage would need to be supplied to the gate of the transfer transistor 14 to turn on transfer transistor 14. In sum, Guidash '656 simply discloses a typical transfer transistor arrangement employing a transistor gate structure for transferring charge from photodiode 12 to sense node 24, and neither discloses nor remotely suggests the pinned transfer gate specified by claim 1. For these reasons, applicant respectfully submits that the rejection of independent claim 1 and its corresponding dependent claims 2-11 has been traversed, and that, therefore, claims 1-11 should now be allowed.

Claims 1-6.

The Examiner has rejected claims 1-6 under 35 USC §102(e) as being anticipated by U.S. patent application publication 2002/0121655 to Zheng, et al. ("Zheng '655"). For the reasons discussed below, applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Zheng '655. However, applicant reserves the right to provide declarations and/or documents under 37 CFR §1.131 to "swear behind" the effective filing date of Zheng '655.

Subject to applicant's reserved right to establish priority of the present invention under 37 CFR §1.131, applicant submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Zheng '655.

With respect to Figure 1 of Zheng '655, a transistor (identified as "p-MOSFET" in Zheng '655) is used to transfer charge collected by photodiode 22. As such, p-MOSFET

includes a transistor gate structure (shown but not designated with a reference number in Figure 1 of Zheng '655) situated between source and drain regions of the p-MOSFET. For similar reasons discussed above in conjunction with Guidash '655, p-MOSFET shown in Figure 1 of Zheng '655 cannot be a pinned transfer gate as specified by claim 1, since it includes a transistor gate structure, which must be enabled to transfer charge from photodiode 22 to a sense node.

Similarly, with respect to Figure 5 of Zheng '655, SIO transistor 83, functioning as a transfer transistor, includes a transistor gate structure (shown but not designated with a reference number in Figure 5 of Zheng '655) situated between source and drain regions. As such, silicon-on-insulator ("SIO") transistor 83 cannot be a pinned transfer gate as specified by claim 1, since it includes a transistor gate structure, which must be enabled to transfer charge from photo-collection area 98 to sense node 96.

Furthermore, neither are the transistor gate structures of p-MOSFET shown in Figure 1 of Zheng '655 and/or SIO transistor 83 shown in Figure 5 of Zheng '655 connected to the same voltage as the substrate. In sum, Zheng '655 simply discloses a typical transfer transistor arrangement employing a transistor gate structure for transferring charge from a photodiode to a sense node, and neither discloses nor remotely suggests the pinned transfer gate specified by claim 1. For these reasons, applicant respectfully submits that the rejection of independent claim 1 and its corresponding dependent claims 2-11 has been traversed, and that, therefore, claims 1-11 should now be allowed.

F. **Rejection of Claims 9-34 and 58-71 Under 35 USC §103**

Claim 9-11.

The Examiner has rejected dependent claims 9-11 under 35 USC §103(a) as being unpatentable over Zheng '655 in view of Turko, et al. (USPN 5,121,214) ("Turko '214"). As discussed above, independent claim 1 is patentably distinguishable over Zheng '655 and, as such, claims 9-11 depending from independent claim 1, are, a fortiori, also patentably distinguishable over Zheng '655. Accordingly, claims 9-11 are patentably distinguishable over Zheng '655 in view of Turko '214.

Claims 12-34 and 58-71.

The Examiner has rejected claims 12-34 and 58-71 under 35 USC §103(a) as being unpatentable over Guidash '656. Applicant respectfully disagrees; however, in order to expedite the prosecution of the present application, applicant has amended independent claims 12, 23, 58, 70 and 71 to specify limitations analogous to those specified by independent claim 1. As discussed above, independent claim 1 is patentably distinguishable over Guidash '656. Accordingly, applicant respectfully submits that independent claims 12, 23, 58, 70 and 71, and their corresponding dependent claims 13-22, 24-34 and 59-69 are allowable over Guidash '656 for at least the same reasons claim 1 is allowable over Guidash '656, as discussed above.

Claims 12-34 and 58-71.

The Examiner has rejected claims 12-34 and 58-71 under 35 USC §103(a) as being unpatentable over Zheng '655. Applicant respectfully disagrees; however, in order to expedite the prosecution of the present application, applicant has amended independent

claims 12, 23, 58, 70 and 71 to specify limitations analogous to those specified by independent claim 1. As discussed above, independent claim 1 is patentably distinguishable over Zheng '655. Accordingly, applicant respectfully submits that independent claims 12, 23, 58, 70 and 71, and their corresponding dependent claims 13-22, 24-34 and 59-69 are allowable over Zheng '655 for at least the same reasons claim 1 is allowable over Zheng '655, as discussed above.

G. Conclusion

For all the foregoing reasons, an early allowance of claims 1-34 and 58-71 pending in the present application is respectfully requested.

Respectfully Submitted;
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